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EXAMINER	
LI, AIMEE J	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/713,441	Applicant(s) BOSSHART, PATRICK W.	
	Examin r Aimee J Li	Art Unit 2183	

-- Th MAILING DATE of this communication appears on the cover sh et with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 December 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-21 and new claim 22 have been considered. Claims 1, 3, 5-9, 16-18, and 20 have been amended as per Applicant's request. New claim 22 has been added as per Applicant's request.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-5, 10-12, and 16 are rejected under 35 U.S.C. 102(b) as being taught by Yung, U.S. Patent Number 5,809,324 (herein referred to as Yung).

4. Referring to claim 1, Yung has taught a processor having a changeable architected state, comprising:

a. Instruction memory for storing instructions (Yung Abstract; column 2, lines 55-62; and Figure 1);

b. An instruction pipeline, wherein an instruction which passes entirely through the pipeline alters the architected state and wherein the pipeline comprises circuitry for fetching instructions from the instruction memory into the pipeline (Yung column 1, lines 7-18; column 4, lines 10-38; and Figure 3);

c. Circuitry for storing an annul code having an annul bit corresponding to each instruction of a group of instructions in the pipeline (Yung Abstract; column 2, lines 18-30; column 3, lines 16-18 and 47-56; column 4, lines 7-18 and 39-64;

column 5, lines 40-54; column 6, lines 25-35 and 43-58; Figure 1; and Figure 3); and

d. Circuitry for preventing one or more selected instructions in the group from altering the architected state in response to the corresponding annul bit of the annul code (Yung Abstract; column 2, lines 18-30; column 3, lines 16-18 and 47-56; column 4, lines 7-18 and 39-64; column 5, lines 40-54; column 6, lines 25-35 and 43-58; Figure 1; and Figure 3).

5. Referring to claim 2, Yung has taught

a. Wherein the instruction pipeline further comprises a plurality or execution units (Yung column 1, lines 7-18; column 3, lines 7-12; and Figure 1); and

b. Wherein one of more the plurality of execution units receives a corresponding instruction for executing the corresponding instruction in a given clock cycle (Yung column 1, lines 7-18; column 3, lines 7-12; and Figure 1).

6. Referring to claim 3, Yung has taught

a. Wherein each annul bit of the annul code comprises either of a first state or a second state (Yung column 2, lines 18-30 and Figure 3);

b. Wherein the circuitry for preventing one or more selected instructions in the group from altering the architected state comprises circuitry for coupling annul bits to respective ones of the plurality of execution units (Yung column 2, lines 18-30; column 3, lines 47-56; column 4, lines 7-18 and 39-64; column 5, lines 40-54; column 6, lines 25-35 and 43-58; Figure 1; Figure 3; and Figure 5);

c. Wherein in response to an annul bit being a first state the execution unit to which the annul bit is coupled does not execute the corresponding instruction in the given clock cycle (Yung Abstract; column 2, lines 18-30; column 3, lines 16-18 and 47-56; column 4, lines 7-18 and 39-64; column 5, lines 40-54; column 6, lines 25-35 and 43-58; Figure 1; Figure 3; and Figure 5); and

d. Wherein in response to an annul bit being a second state different than the first state the execution unit to which the annul bit is coupled does execute the corresponding instruction in the given clock cycle (Yung Abstract; column 2, lines 18-30; column 3, lines 16-18 and 47-56; column 4, lines 7-18 and 39-64; column 5, lines 40-54; column 6, lines 25-35 and 43-58; Figure 1; Figure 3; and Figure 5).

7. Referring to claim 4, Yung has taught wherein the plurality of execution units comprises a load/store unit, a multiply unit, an ALU unit, and a shift unit (Yung column 3, lines 7-12 and Figure 1).

8. Referring to claim 5, Yung has taught

a. Wherein the plurality of execution units are operable such that in a given clock cycle an integer number N of the plurality of execution units are scheduled to execute (Yung column 3, lines 7-12 and Figure 1); and

b. Wherein the circuitry for coupling the annul bits to respective ones of the plurality of execution units comprises circuitry for coupling only the integer number N of the annul bits to the plurality of execution units which are scheduled to execute in the given clock cycle (Yung Abstract; column 2, lines 18-30; column 3, lines 16-

18 and 47-56; column 4, lines 7-18 and 39-64; column 5, lines 40-54; column 6, lines 25-35 and 43-58; Figure 1; Figure 3; and Figure 5).

9. Referring to claim 10, Yung has taught wherein the annul code is generated in response to one or more constant generating instructions (Yung Abstract; column 2, lines 18-30; column 3, lines 16-18 and 47-56; column 4, lines 7-18 and 39-64; column 5, lines 40-54; column 6, lines 25-35 and 43-58; Figure 1; Figure 3; and Figure 5).

10. Referring to claim 11, Yung has taught wherein the annul code is loaded from a memory (Yung Abstract; column 2, lines 18-30; column 3, lines 16-18 and 47-56; column 4, lines 7-18 and 39-64; column 5, lines 40-54; column 6, lines 25-35 and 43-58; Figure 1; Figure 3; and Figure 5).

11. Referring to claim 12, Yung has taught wherein the annul code is an immediate value in an instruction passing through the pipeline (Yung Abstract; column 2, lines 18-30; column 3, lines 16-18 and 47-56; column 4, lines 7-18 and 39-64; column 5, lines 40-54; column 6, lines 25-35 and 43-58; Figure 1; Figure 3; and Figure 5).

12. Referring to claim 16, Yung has taught

a. Wherein the annul code is loaded in response to an instruction having a condition predicate (Yung column 1, lines 24-47). In regards to Yung, it is inherent that the branch is a type of predicate instruction, since the condition portion of the instruction is affirmed or denied. For the definition of "predicate" please see American Heritage® Dictionary of the English Language under Predicate.

b. Wherein the annul code comprises a first annul code loaded in response to the condition predicate being satisfied (Yung Abstract; column 2, lines 18-30; column

3, lines 16-18 and 47-56; column 4, lines 7-18 and 39-64; column 5, lines 40-54; column 6, lines 25-35 and 43-58; Figure 1; and Figure 3); and

c. Wherein the annul code comprises a second annul code loaded in response to the condition predicate not being satisfied (Yung Abstract; column 2, lines 18-30; column 3, lines 16-18 and 47-56; column 4, lines 7-18 and 39-64; column 5, lines 40-54; column 6, lines 25-35 and 43-58; Figure 1; and Figure 3).

Claim Rejections - 35 USC § 103

13. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

14. Claims 6, 9, and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yung, U.S. Patent Number 5,809,324 (herein referred to as Yung), as applied to claims 3 and 5 for claims 9 and 6 respectively, in view of Lass, U.S. Patent Number 5,165,025 (herein referred to as Lass).

15. Referring to claims 6 and 9, Yung has taught

a. Wherein the instructions corresponding to the annul code comprise:

i. A first group of one or more instructions logically arranged after a conditional instruction and to be executed if the condition is satisfied (Applicant's claims 6 and 9) (Yung column 1, lines 35-47; column 2, lines 15-30 and 55-62; and column 3, lines 40-56);

b. Wherein the circuitry for preventing prevents the first group of instructions from altering the architected state in response to corresponding annul bits of the annul code having the first state if the condition is not satisfied (Applicant's claim 6) (Yung Abstract; column 2, lines 18-30; column 3, lines 16-18 and 47-56; column 4, lines 7-18 and 39-64; column 5, lines 40-54; column 6, lines 25-35 and 43-58; Figure 1; and Figure 3);

c. Wherein the circuitry for preventing prevents a group of instructions from altering the architected state in response to corresponding annul bits of the annul code having the first state if the condition is satisfied (Applicant's claim 6) (Yung Abstract; column 2, lines 18-30; column 3, lines 16-18 and 47-56; column 4, lines 7-18 and 39-64; column 5, lines 40-54; column 6, lines 25-35 and 43-58; Figure 1; and Figure 3);

d. Wherein the annul bits corresponding to the first group of one or more instructions are set to the first state and the annul bits corresponding to the second group of one or more instructions are set to the second state if the condition is not satisfied (Applicant's claim 9) (Yung Abstract; column 2, lines 18-30; column 3, lines 16-18 and 47-56; column 4, lines 7-18 and 39-64; column 5, lines 40-54; column 6, lines 25-35 and 43-58; Figure 1; and Figure 3); and

e. Wherein the annul bits corresponding to the first group of one or more instructions are set to the second state and the annul bits corresponding to the second group of on or more instructions are set to the first state if the condition is satisfied (Yung Abstract; column 2, lines 18-30; column 3, lines 16-18 and 47-56;

column 4, lines 7-18 and 39-64; column 5, lines 40-54; column 6, lines 25-35 and 43-58; Figure 1; and Figure 3).

16. Yung has not explicitly taught a second group of one or more instructions logically arranged after the conditional instruction and to be executed if the condition is not satisfied. However, Yung has taught that all instructions being executed in the pipeline have information stored in the FIFO, including whether the instruction is valid or not (Yung column 3, lines 16-17; column 4, lines 4-64; and Figure 3). Lass has explicitly taught a second group of one or more instructions logically arranged after the conditional instruction and to be executed if the condition is not satisfied (Lass Abstract and column 2, lines 5-13). A person of ordinary skill in the art at the time the invention was made would have recognized that, and as taught by Lass, incorporating fetching second group of instructions would minimize delays due to mispredicted branches (Lass column 2, lines 1-2), thereby increasing processing speed. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate fetching the second group of instructions, as taught by Lass, in the device of Yung to increase processor speed.

17. Referring to claim 22, Yung has taught a method of data processing comprising the steps of:

a. Identifying a group of instructions including a tree of a plurality of conditional branch instructions (Yung Abstract; column 2, lines 55-62; and Figure 1);

b. For each conditional branch instruction within the group of instructions

i. Forming a first annul code having an annul bit corresponding to each instruction following the conditional branch instruction, the annul bit

having a first logical state for instructions following the detected conditional branch instruction executed if a condition of the conditional branch instruction is satisfied and a second logical state opposite to the first logical state for instructions following the detected condition conditional branch instruction executed if the of the conditional branch instruction is not satisfied (Yung Abstract; column 2, lines 18-30; column 3, lines 16-18 and 47-56; column 4, lines 7-18 and 39-64; column 5, lines 40-54; column 6, lines 25-35 and 43-58; Figure 1; and Figure 3),

ii. Forming a second annul code having an annul bit corresponding to each instruction following the conditional branch instruction (Yung Abstract; column 2, lines 18-30; column 3, lines 16-18 and 47-56; column 4, lines 7-18 and 39-64; column 5, lines 40-54; column 6, lines 25-35 and 43-58; Figure 1; and Figure 3) (Lass Abstract and column 2, lines 5-13);

c. Upon execution of the group of instructions

i. Detecting each conditional branch instruction (Yung Abstract; column 2, lines 55-62; column 3, lines 20-62; and Figure 1),

ii. Evaluating the condition of the conditional branch instruction (Yung Abstract; column 2, lines 55-62; and Figure 1),

iii. Loading the corresponding first annul code if the condition of the conditional branch instruction is satisfied (Yung Abstract; column 2, lines 18-30; column 3, lines 16-18 and 47-56; column 4, lines 7-18 and 39-64;

column 5, lines 40-54; column 6, lines 25-35 and 43-58; Figure 1; and Figure 3),

iv. Loading the corresponding second annul code if the condition of the conditional branch instruction is not satisfied (Yung Abstract; column 2, lines 18-30; column 3, lines 16-18 and 47-56; column 4, lines 7-18 and 39-64; column 5, lines 40-54; column 6, lines 25-35 and 43-58; Figure 1; and Figure 3),

v. Executing each instruction following the conditional branch instruction if the corresponding annul bit of the corresponding annul code has the first state (Yung Abstract; column 2, lines 18-30; column 3, lines 16-18 and 47-56; column 4, lines 7-18 and 39-64; column 5, lines 40-54; column 6, lines 25-35 and 43-58; Figure 1; and Figure 3), and

vi. Not executing each instruction following the conditional branch instruction if the corresponding annul bit of the corresponding annul bode has the second state (Yung Abstract; column 2, lines 18-30; column 3, lines 16-18 and 47-56; column 4, lines 7-18 and 39-64; column 5, lines 40-54; column 6, lines 25-35 and 43-58; Figure 1; and Figure 3).

18. Yung has not explicitly taught the annul bit having the second logical state for instructions following the detected conditional branch instruction executed if a condition of the conditional branch instruction is satisfied and the first logical state for instructions following the detected conditional branch instruction executed if the condition of the conditional branch instruction is not satisfied. However, Yung has taught that all instructions being executed in the

pipeline have information stored in the FIFO, including whether the instruction is valid or not (Yung column 3, lines 16-17; column 4, lines 4-64; and Figure 3). Lass has explicitly taught fetching a group of instructions that are not valid if a condition of the conditional branch instruction is satisfied and valid if the condition of the conditional branch instruction is not satisfied (Lass Abstract and column 2, lines 5-13). A person of ordinary skill in the art at the time the invention was made would have recognized that, and as taught by Lass, incorporating fetching second group of instructions would minimize delays due to mispredicted branches (Lass column 2, lines 1-2), thereby increasing processing speed. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate fetching the second group of instructions, as taught by Lass, in the device of Yung to increase processor speed.

19. Claims 7-8, 17, and 20-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yung, U.S. Patent Number 5,809,324 (herein referred to as Yung), as applied to claims 1, 3, 5, and 16, in view of InstantWeb's Free On-line Computing Dictionary ©1995-1999 (herein referred to as InstantWeb).

20. Referring to claims 7 and 8, Yung has taught wherein during a given iteration the circuitry for preventing prevents one or more of the instructions corresponding to the annul bits of the annul code from altering the architected state in response to the annul bits of the annul code (Yung Abstract; column 2, lines 18-30; column 3, lines 16-18 and 47-56; column 4, lines 7-18 and 39-64; column 5, lines 40-54; column 6, lines 25-35 and 43-58; Figure 1; and Figure 3). Yung has not explicitly taught

a. A software loop scheduled to execute for an integer M number of iterations; and

b. The annul bits of the annul code are based on a relationship of the given iteration to the integer M number of iterations.

21. However, Yung has taught that the annul code comprise and are based upon branch instructions (Yung Abstract; column 2, lines 18-30; column 3, lines 16-18 and 47-56; column 4, lines 7-18 and 39-64; column 5, lines 40-54; column 6, lines 25-35 and 43-58; Figure 1; and Figure 3). InstantWeb has taught

a. A software loop scheduled to execute for an integer M number of iterations (InstantWeb Loop; Repeat Loop; While; Jump); and

b. The annul bits of the annul code are based on a relationship of the given iteration to the integer M number of iterations (InstantWeb Loop; Repeat Loop; While; Jump).

22. In regards to InstantWeb, loops are synthesized with jump, or branch, instructions (InstantWeb Loop). A person of ordinary skill in the art at the time the invention was made would have recognized, and as taught by InstantWeb, software loops are a type of branch instruction (InstantWeb Loop). Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate the software loops of InstantWeb in the device of Yung.

23. Referring to claim 17, Yung has taught

a. Wherein the first annul code is stored (Yung column 6, lines 51-53); and

b. Wherein the second annul code is stored (Yung column 6, lines 51-53).

24. Yung has not explicitly taught a first data register and a second data register. However, Yung has taught that the first and second annul code must be stored in some memory apparatus

(Yung column 6, lines 51-53). InstantWeb has explicitly taught registers (InstantWeb Register). A person of ordinary skill in the art at the time the invention was made, and as taught by InstantWeb, would have recognized that registers allow for data to be retrieved faster (InstantWeb Register), thereby increasing the speed of the processor. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate the registers of InstantWeb in the device of Yung to increase processor speed.

25. Referring 20, Yung has taught

a. Storing the annul code which comprises a set of annul bits having a first logical value and a set of annul bits having a second logical value (Yung Abstract; column 2, lines 18-30; column 3, lines 16-18 and 47-56; column 4, lines 7-18 and 39-64; column 5, lines 40-54; column 6, lines 25-35 and 43-58; Figure 1; and Figure 3);

b. Wherein the annul code is loaded in response to an instruction having a condition predicate (Yung column 1, lines 24-47). In regards to Yung, it is inherent that the branch is a type of predicate instruction, since the condition portion of the instruction is affirmed or denied. For the definition of "predicate" please see American Heritage® Dictionary of the English Language under Predicate.

c. Wherein the circuitry for preventing prevents instructions corresponding to annul bits having a first logical value from altering the architected state in response to the condition predicate being satisfied (Yung Abstract; column 2, lines 18-30; column 3, lines 16-18 and 47-56; column 4, lines 7-18 and 39-64; column 5, lines 40-54; column 6, lines 25-35 and 43-58; Figure 1; and Figure 3); and

d. Wherein the circuitry for preventing prevents instructions corresponding to annul bits having a second logical value opposite the first logical state from altering the architected state in response to the condition predicate not being satisfied (Yung Abstract; column 2, lines 18-30; column 3, lines 16-18 and 47-56; column 4, lines 7-18 and 39-64; column 5, lines 40-54; column 6, lines 25-35 and 43-58; Figure 1; and Figure 3).

26. Yung has not explicitly taught a data register. However, Yung has taught that the first and second annul code must be stored in some memory apparatus (Yung column 6, lines 51-53). InstantWeb has explicitly taught registers (InstantWeb Register). A person of ordinary skill in the art at the time the invention was made, and as taught by InstantWeb, would have recognized that registers allow for data to be retrieved faster (InstantWeb Register), thereby increasing the speed of the processor. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate the registers of InstantWeb in the device of Yung to increase processor speed.

27. Referring to claim 21, Yung has not taught circuitry for storing a portion of the annul code in response to receipt of an interrupt. InstantWeb has taught circuitry for storing a portion of the annul code in response to receipt of an interrupt (InstantWeb Interrupt). In regards to InstantWeb, saving the current state of the running program includes saving data in the current associated memories, which includes the FIFO. A person of ordinary skill in the art at the time the invention was made would have recognized that saving the current state saves the current status of the system, thereby minimizing the risk for data corruption. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to

incorporate saving the current state of InstantWeb in the device of Yung to minimize data corruption.

28. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yung, U.S. Patent Number 5,809,324 (herein referred to as Yung), as applied to claim 16, in view of Brender, U.S. Patent Number 3,638,195 (herein referred to as Brender). Yung has taught storing the first and second annul code (Yung column 6, lines 51-53). Yung has not explicitly taught

a. A data register (Brender column 3, lines 8-13);

b. Storing data in a first one-half of the data register (Brender column 3, lines 8-13); and

c. Storing data in a second one-half of the data register different from the first one-half (Brender column 3, lines 8-13).

29. However, Yung has taught that the first and second annul code must be stored in some memory apparatus (Yung column 6, lines 51-53). Brender has explicitly taught

a. A data register (Brender column 3, lines 8-13);

b. Storing data in a first one-half of the data register (Brender column 3, lines 8-13); and

c. Storing data in a second one-half of the data register different from the first one-half (Brender column 3, lines 8-13).

30. A person of ordinary skill in the art at the time the invention was made, and as taught by Brender, would have recognized that the registers allow for data to be retrieved independently and in parallel (Brender column 3, lines 8-13), thereby increasing the speed of the processor by reducing allowing more data to be accessed at once. Therefore, it would have been obvious to a

person of ordinary skill in the art at the time this invention was made to incorporate the registers of Brender in the device of Yung to increase processor speed.

31. Claims 13-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yung, U.S. Patent Number 5,809,324 (herein referred to as Yung) in view of *In re Rose*, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); *In re Rinehart*, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976), and *In Gardner v. TEC Systems, Inc.*, 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984) cert. denied, 469 U.S. 830, 225 USPQ 232 (1984) (herein referred to In re Rose). In regards to In re Rose, all cases pertain towards changes in size and proportion as a non-patentable feature and are referred to in the MPEP 1244.04. Yung has not taught wherein the annul code is formed in response to two thirty-two bit values (Applicant's claim 15) (Yung column 3, lines 19-41). Yung has not explicitly taught

a. Wherein the annul code comprises 32 bits (Applicant's claim 13);

b. Wherein the annul code comprises more than 32 bits (Applicant's claim 14); and

c. Wherein the annul code comprises 64 bits (Applicant's claim 15).

32. However, Yung has taught that the annul code exists and is used (Yung Abstract; column 2, lines 18-30; column 3, lines 16-18 and 47-56; column 4, lines 7-18 and 39-64; column 5, lines 40-54; column 6, lines 25-35 and 43-58; Figure 1; and Figure 3). In re Rose has taught that changes in size and proportion of an invention are not a patentable feature when the function of the device remains the same. In this case, merely changing the size of the annul code is not a patentable distinction, since the device functions the same no matter the size of the annul code. No matter the size of the annul code, Yung's device will annul instructions according to the information stored in the annul code.

33. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yung, U.S. Patent Number 5,809,324 (herein referred to as Yung) in view of Dubey et al., U.S. Patent Number 5,812,811 (herein referred to as Dubey). Yung has not explicitly taught

a. Wherein an annul instruction passing through the pipeline specifies an integer N; and

b. Wherein the annul code is formed in response to the integer value N such that the circuitry for preventing prevents N successive instructions in the pipeline from altering the architected state.

34. However, Yung has taught that all instructions being executed in the pipeline have information stored in the FIFO, including whether the instruction is valid or not, and that the instruction valid information is altered depending on the status of that instruction (Yung column 3, lines 16-17; column 4, lines 4-64; and Figure 3). Dubey has taught

a. Wherein an annul instruction passing through the pipeline specifies an integer N (Dubey column 6, lines 13-19; column 9, lines 29-35; column 10, lines 12-36; column 12, lines 28-33; column 12, line 52 to column 13, line 3; Figure 3E; Figure 3H; and Figure 3I); and

b. Wherein the annul code is formed in response to the integer value N such that the circuitry for preventing prevents N successive instructions in the pipeline from altering the architected state (Dubey column 6, lines 13-19; column 9, lines 29-35; column 10, lines 12-36; column 12, lines 28-33; column 12, line 52 to column 13, line 3; Figure 3E; Figure 3H; and Figure 3I).

35. A person of ordinary skill in the art at the time the invention was made, and as taught by Dubey, would have recognized that incorporating the annul instruction would reduce or eliminate execution of redundant instructions (Dubey column 13, lines 58-65), thereby increasing processor efficiency and speed. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the annul instruction of Dubey in the device of Yung to increase processor efficiency and speed.

Response to Arguments

36. Examiner withdraws the objection to the title in favor of the amended title.

37. Examiner withdraws the objection to the abstract in favor of the amended abstract.

38. Applicant's arguments with respect to claims 1-22 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

39. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure as follows. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

a. Wilkes, U.S. Patent Number 4,439,827, has taught a processor which fetches both the predicted branch path and the fall-through path and indicates which is to be executed.

b. Bruckert et al., U.S. Patent Number 4,742,451, has taught a processor which fetches both the predicted branch path and the fall-through path and indicates which is to be executed.

c. Denman, Jr., U.S. Patent Number 5,493,669, has taught distinguishing valid and invalid instructions.

d. Tremblay et al., U.S. Patent Number 5,748,935, has taught distinguishing valid and invalid instructions.

e. Leung et al., U.S. Patent Number 5,784,603, has taught distinguishing valid and invalid instructions.

f. Lesartre, U.S. Patent Number 5,799,167, has taught a processor which fetches both the predicted branch path and the fall-through path and indicates which is to be executed.

g. Arnold et al., U.S. Patent Number 6,512,706, has taught predicate instructions with validity bits.

40. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

41. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

42. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J Li whose telephone number is (703) 305-7596. The examiner can normally be reached on M-T 7:30am-5:00pm.

43. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

44. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Aimee J. Li
Examiner
Art Unit 2183

February 20, 2004

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100